REMARKS

This Amendment is filed in response to the Office Action dated Oct. 3rd, 2003. All objections and rejections are respectfully traversed.

Claims 1, 11, 12, 15, 19, and 20 have been amended to better claim the invention

New claims 21-34 have been added.

Claims 1-34 are now pending in the case.

Objection to the Abstract

At paragraph 1 the abstract was objected to as containing more than 150 words. The Applicant has deleted words from the abstract to reduce the word count.

Rejections under 35 U.S.C. §112

At paragraph 3 of the Office Action claims 12-18 were rejected under 35 U.S.C. §112 as failing to comply with the enablement requirement. The Examiner recounts that claim 12 claims a "last counter" and claim 15 claims a "current counter", and asserts that "neither claim enables one to understand the function of these two counters."

While the Applicant has amended some of these claims to make them more clear, the Applicant respectfully holds that the rejection under 35 U.S.C. §112 was improper and that the claims should have been allowable in original form.

35 U.S.C. §112, first paragraph requires the "*specification* shall contain a written description of the invention", *not* that each and every *claim* must contain a full written description. See MPEP §2163. Further, the Applicant is allowed to be his own lexicographer. See MPEP §2111.01. Pursuant to this, Applicant has defined "last counter" and "current counter" in the specification in great detail. At page 14, line 28 to page 15, line 5, in reference to Fig 5, the specification teaches:

> ... a first counter (e.g., ***current counter*** 566) is provided in the FPGA 560 that counts the interrupt pulses generated by the DMA controller 550 as they are received at the device 560. The FPGA preferably maintains a ***current counter*** for each interupt signal, 554, 556 and increments that counter every time an interup pulse (i.e. an actie edge) is detected. The counter 566 "wraps" to an initialized value, e.g., 0, whenever it reaches its maximum value, which is illustratively 16 bits.

And at page 15, lines 13-16, in reference to Fig 5, the specification teaches:

> ... a second counter (e.g., a last counter 514) is provided in the CPU 510 that is incremented in response to each interrupt service by the CPU. In other words, after processing each CPU-owned control block 524, the interrupt handler 512 increments the last counter 514.

It is therefore proper for the Applicant to refer to a "last counter" and a "current counter" without additional description, as these terms should be read in light of the text of the specification.

Rejections under 35 U.S.C. §102

At paragraph 4-5 of the Office Action claims 1, 7, 11, and 19-20 were rejected under 35 U.S.C. §102 as being anticipated by Greim et al. U.S Patent No. 6,163,829 (hereinafter Greim).

The Applicant's present invention, as set forth in representative claim 1 comprises in part:

> A system configured to acknowledge and service an interrupt issued to a processor of an intermediate node, the system comprising:
> an external device coupled to a high latency path, ***the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;***
> an interrupt multiplexing device accessible by the processor over a fast bus, ***the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device;***
> a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and
> a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,
> wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus.

Greim teaches a system for interrupt handling in a multiprocessor computer where interrupt signals are directed to the appropriate processor by an interrupt distribution logic unit. First, a generic interrupt signal (INT 4) alerts the processor that an interrupt is pending. Then, the processor accesses stored information about the pending interrupt by reading registers over a local bus (Fig 6, item 22) and services the pending interrupt (col.

29, lines 10-26). Finally, an interrupt acknowledge block (fig 5, item 162) generates an conventional acknowledgement signal on the system bus to clear the pending interrupt and indicate completion (col. 29, line 36 – col. 30, line 3).

The Applicant respectfully urges that Greim does not show the Applicant's claimed invention relating to ***"the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor"*** and ***"the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device."*** The present invention uses "***pulsed interrupt signals***," that is, "the DMA controller asserts an interrupt by 'pulsing' an appropriate interrupt signal to [a] device to thereby obviate the need to acknowledge and clear the interrupt signals" (specification page 14, lines 2-4). The novel use of pulsed signals presents technical challenges (such as the possibility of missed interrupts) that other aspects of the present invention innovatively solve. Greim contains absolutely no suggestion of pulsed interrupt signals. Indeed, Greim teaches the use of acknowledge signals over a slow system bus, the type of slow operation the present invention is directed to overcome. Accordingly, the Applicant respectfully urges that Greim does not anticipate the present invention under 35 U.S.C. §102 because of the absence of the claimed novel ***"external device generating a pulsed interrupt signal for each type of interrupt supported by the processor"*** and ***"the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device."***

Rejections under 35 U.S.C. §103

At paragraph 6-8 of Office Action claims 2-6 and 12-17 were rejected under 35 U.S.C. §103 as being unpatentable over the combination of Greim and Shek et al. U.S. Patent No. 6,185,652 (hereinafter Shek).

Shek teaches an interrupt generator, that receives tasks from a cpu, increments an interrupt counter, generates interrupts for the tasks, and then directs these interrupts back to the same cpu (col 4, lines 10-18). Verification (acknowledgement) is accomplished through comparison schemes between expected and issued interrupts (col. 4, lines 38-53).

Claims 2-6 and 12-17 are dependant claims that depend upon allowable independent claims. Therefore, the Applicant respectfully urges that the combination of Greim and Shek does not render the claims obvious under 35 U.S.C. §103.

At paragraph 9 of Office Action claim 18 was rejected under 35 U.S.C. §103 as being unpatentable over the combination of Greim, Shek and Ecclesine, U.S. Patent No. 5,983,275 (hereinafter Ecclesine).

Ecclesine teaches a system for providing conventional interrupts to a processor to drive a data frame receiver function.

Claims 18 is a dependant claim that depends upon an allowable independent claim. Therefore, the Applicant respectfully urges that the combination of Greim and Shek and Ecclesine does not render the claim obvious under 35 U.S.C. §103.

At paragraph 10 of Office Action claims 8-10 were rejected under 35 U.S.C. §103 as being unpatentable over the combination of Greim and "design choice."

Claims 8-10 are dependant claims that depend upon allowable independent claims. Therefore, the Applicant respectfully urges that the combination of Greim and design does not render the claims obvious under 35 U.S.C. §103.

At paragraph 11 of Office Action claims 1, 7, and 19-20 were rejected under 35 U.S.C. §103 as being unpatentable over the combination of Swanstrom, U.S Patent No. 5,754,884 (hereinafter Swanstrom) and Greim.

Swanstrom discloses an interrupt servicing DMA controller connected to a CPU through a Peripheral Interrupt Controller (fig 1, item 160). The CPU issues conventional acknowledge signal over a high latency path to clear pending interrupts and indicate completion (col. 8, lines 22-24).

Among other things, Swanstrom makes absolutely no suggestion of the Applicant's claimed novel "***external device generating a pulsed interrupt signal for each type of interrupt supported by the processor***" and "***the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device***." Indeed Swanstrom teaches using conventional acknowledge signals over a slow path. Therefore, the Applicant respectfully urges that

the combination of Swanstrom and Greim does not render the Applicant's claimed invention obvious under 35 U.S.C. §103.

At paragraph 12 of Office Action claims 2-6 and 12-18 were rejected under 35 U.S.C. §103 as being unpatentable over the combination of Swanstrom, Greim and Shek.

Claims 2-6 and 12-18 are dependant claims that depend upon allowable independent claims. Hence, the Applicant respectfully urges that the combination of Swanstrom, Greim, and Shek does not render the claims obvious under 35 U.S.C. §103.

At paragraph 13 of Office Action claims 8-10 were rejected under 35 U.S.C. §103 as being unpatentable over the combination of Swanstrom, Greim, and "design choice."

Claims 8-10 are dependant claims that depend upon allowable independent claims. Therefore, the Applicant respectfully urges that the combination of Swanstrom, Greim, and Shek does not render the Applicant's claimed invention obvious under 35 U.S.C. §103.

At paragraph 14 of Office Action claim 18 was rejected under 35 U.S.C. §103 as being unpatentable over the combination of Swanstrom, Greim, Shek and Ecclesine.

Claims 18 is a dependant claim that depends upon an allowable independent claims. Accordingly, the Applicant respectfully urges that the combination of Swanstrom, Greim, Shek, Ecclesine does not render the claim obvious under 35 U.S.C. §103.

All independent claims are believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

The Applicant respectfully solicits favorable action.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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